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EXAMINER HUBER, ROBERT T				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/522,502

Applicant(s)

ERTLE ET AL.

Examiner

ROBERT HUBER

Art Unit

2892

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 18, 19, 22-39, 41 and 42 is/are pending in the application.
- 4a) Of the above claim(s) 34-37 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 18, 19, 22-33, 38, 39, 41, 42 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 July 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The Examiner acknowledges the amendment(s) to claims 18, 28, 38, and 39 filed on July 1, 2009. The rejection of claim(s) 18, 19, 22 – 33, 38, 39, and 41 under USC 112, second paragraph, cited in the previous office action filed on April 6, 2009 is (are) hereby withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 18, 26 – 28, 38, 39, 41, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 6,159,826, prior art of record) in view of Strauss (US 5,719,449).

a. Regarding claim 18, **Kim discloses a semiconductor chip** (e.g. figures 4 and 5) **comprising:**

a passive first region on a top side of the semiconductor chip (region 34);

an active second region on the top side of the semiconductor chip (region 32);

an arrangement of contact areas (contact areas 56b) **and test areas** (test areas 56a) **having respective top surfaces which are arranged in a common plane** (e.g. as seen in figure 5, the top surfaces of the contact and test areas are in a common plane) **and exposed to the top side of the semiconductor chip through contact windows and test windows** (windows formed by the absence of layer 57 on the substrate), **respectively, the contact areas and test areas are in each case electrically conductively connected to one another via a conduction web that has a top surface that lies in the common plane** (e.g. conducting web 56, which has a top surfaces that is in the common plane as the test areas and contact areas 56a and 56b), **the contact areas being arranged in the passive first region** (contact areas 56b are in the passive region 34), **the passive first region having no active components of an integrated circuit** (as seen in figure 5, there are no active devices in this

region), **the test areas being arranged in the active second region** (test areas 56a are in the active region 32), **the active second region having active components of an integrated circuit** (e.g. as seen in figure 5, the active second region has P+ and N+ regions, which are components of an integrated circuit); **and**

an insulating layer situated between the top side and a lower plane (insulating layer 53, disclosed in col. 3, line 33);

through contacts extending through a portion of the insulation layer below the conduction web (through contacts 55) **and extending from the conduction web to a lower plane** (as seen in figure 5), **the through contacts being connected to interconnects** (interconnects 52a and 52) **that are connected to electrodes of the components of the integrated circuit** (e.g. vias connected to the P+ and N+ regions of region 32, and connected to layers 52a and 52);

wherein portions of the insulating layer directly below the contact areas and the test areas are free from the through contacts (as seen in figure 5, portions of the insulating layer 53 directly below the contact and test areas are free from the through contacts).

Kim is silent with respect to disclosing the through contacts extending through a portion of the insulating layer are directly below the conduction web (the conduction web is interpreted as the layer 56 under the insulating layer 57).

Strauss discloses a semiconductor chip (figure 2) comprising an arrangement of contact areas (contact areas 224) and test areas (test areas 222) having respective top surfaces which are arranged in a common plane (e.g. as seen in figure 2, the top surfaces of the contact and test areas are in a common plane) and exposed to the top side of the semiconductor chip through contact windows and test windows (windows formed by the absence of layer 219/220/221 on the substrate), respectively, the contact areas and test areas are in each case electrically conductively connected to one another via a conduction web that has a top surface that lies in the common plane (e.g. conducting web of layer 217 under the layer 220, which has a top surfaces that is in the common plane as the test areas and contact areas 222 and 224); an insulating layer situated between the top side and a lower plane (insulating layer 216); and through contacts extending through a portion of the insulation layer (through contacts 218) directly below the conduction web and extending from the conduction web to a lower plane (as seen in figure 2), the through contacts being connected to interconnects (interconnects 213).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kim such that the through contacts were formed directly below the conduction web since Kim discloses the through contacts to extend below a side of the conduction web, and Strauss discloses that they may be formed directly below the conduction web.

Furthermore, it has been held that rearranging parts of a prior art structure involves only routing skill in the art. *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950). See MPEP 2144.04. One would have been motivated to form the through contact directly below the conduction web in order to avoid damage to the through contact from the formation of a contact on the contact pad.

b. Regarding claim 26, **Kim in view of Strauss disclose the semiconductor chip of claim 18, as cited above, comprising wherein the conduction web is formed in T** (Kim: e.g. as seen in figure 4, a T is formed from the conduction web 36 at the interface of the test areas and contact areas) **having a transverse bar and a longitudinal bar, the transverse bar of the T having a width about equal to the width of the contact areas** (Kim: e.g. as seen in figure 5, the transverse bar of the T has a vertical width of equal to the vertical width of the contact area 56b) **and having through contacts to interconnects** (Kim: through contacts 55 to interconnects 52), **while the longitudinal bar of the T has a width determined in response to the maximum current loading during testing by test tips** (Kim: the claim limitation of "*a width determined in response to the maximum current loading*" is not given patentable weight since the patentability of a product does not depend on the method of production. See MPEP 2113. The width of the longitudinal bar of the T exists and the conduction web is capable of supplying current during testing, therefore the structure anticipates the claimed limitation).

c. Regarding claim 27, **Kim in view of Strauss disclose the semiconductor chip of claim 18, comprising wherein the test areas have a width (b_p) about equal to a width of the contact areas and have a length (l_p) greater than their width (b_p)** (Kim: e.g. as seen in figure 5, the vertical width of the test areas 56a and contact areas 56b are about equal, and the horizontal length of the test areas are greater than the their vertical width).

d. Regarding claim 28, **Kim discloses an electronic device** (e.g. figures 4 and 5) **comprising:**

a semiconductor chip (semiconductor chips 32, disclosed in col. 3, line 8), **the semiconductor chip having an arrangement of contact areas** (contact areas 56b) **and test areas** (test areas 56a) **which are arranged in a common plane** (e.g. as seen in figure 5, the dope surfaces of the contact and test areas are in a common plane) **and are in each case electrically conductively connected to one another via a conduction web that lies in the common plane** (e.g. conducting web 56, which has a top surfaces that is in the common plane as the test areas and contact areas 56a and 56b), **the contact areas being arranged in a passive, first region of a top side of the semiconductor chip** (passive region 34), **the passive first region having no active components of an integrated circuit** (as seen in figure 5, there are no active devices in this region);

the test areas being arranged in an active, second region of the top side of the semiconductor chip (active region 32), the active second region having active components of an integrated circuit (e.g. as seen in figure 5, the active second region has P+ and N+ regions, which are components of an integrated circuit);

the test areas and contact areas being formed in the same interconnect plane (e.g. as seen in figure 5); and

the length (l_p) of the test areas being greater than the width (b_p) thereof (e.g. as seen in figure 5, the vertical length of the test area is greater than the horizontal width); and

an insulating layer situated between a top side and a lower plane (insulating layer 53, disclosed in col. 3, line 33);

through contacts extending through a portion of the insulating layer (through contacts 55) below the conduction web and extending from the conduction web to a lower plane (as seen in figure 5), the through contacts being connected to interconnects (interconnects 52a and 52) that are connected to electrodes of the components of the integrated circuit (e.g. vias connected to the P+ and N+ regions of region 32, and connected to layers 52a and 52);

wherein portions of the insulating layer directly below the contact areas and the test areas are free from the through contacts (as seen in figure

5, portions of the insulating layer 53 directly below the contact and test areas are free from the through contacts).

Kim is silent with respect to explicitly stating that the length (l_p) of the test areas being at least approximately 1.5 times greater than the width (b_p) thereof. However, as seen in figures 6 and 16, the vertical length of the test areas are at least greater than their horizontal width. Although the figures are not indicated to be drawn to scale, it would have been obvious for one of ordinary skill in the art at the time the invention was made to make the structure of Kim such a that the horizontal length of the test areas are at least approximately 1.5 times greater than their vertical width, since often the thickness (vertical width) of the layers are much thinner than the (horizontal) length of the layers, and the figures imply such a configuration for the device. It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make such a modification in order to accommodate a large test probe while having a thin layer in order to minimize device thickness.

Kim is also silent with respect to disclosing the through contacts extending through a portion of the insulating layer are directly below the conduction web (the conduction web is interpreted as the layer 56 under the insulating layer 57).

Strauss discloses a semiconductor chip (figure 2) comprising an arrangement of contact areas (contact areas 224) and test areas (test areas 222) having respective top surfaces which are arranged in a common plane (e.g. as seen in figure 2, the top surfaces of the contact and test areas are in a common plane) and exposed to the top side of the semiconductor chip through contact windows and test windows (windows formed by the absence of layer 219/220/221 on the substrate), respectively, the contact areas and test areas are in each case electrically conductively connected to one another via a conduction web that has a top surface that lies in the common plane (e.g. conducting web of layer 217 under the layer 220, which has a top surfaces that is in the common plane as the test areas and contact areas 222 and 224); an insulating layer situated between the top side and a lower plane (insulating layer 216); and through contacts extending through a portion of the insulation layer (through contacts 218) directly below the conduction web and extending from the conduction web to a lower plane (as seen in figure 2), the through contacts being connected to interconnects (interconnects 213).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kim such that the through contacts were formed directly below the conduction web since Kim discloses the through contacts to extend below a side of the conduction web, and Strauss discloses that they may be formed directly below the conduction web.

Furthermore, it has been held that rearranging parts of a prior art structure involves only routing skill in the art. *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950). See MPEP 2144.04. One would have been motivated to form the through contact directly below the conduction web in order to avoid damage to the through contact from the formation of a contact on the contact pad.

e. Regarding claim 38, **Strauss discloses a semiconductor wafer** (e.g. figures 2 and 3) **comprising:**

a semiconductor chip (chip as seen in figures 2 and 3) **having a passive first region** (first region under wafer probe pad 222, as clarified in the figure below) **and an active second region** (active second region under contact pad 224, as clarified in the figure below), **the semiconductor chip having an arrangement of contact areas** (contact areas 222) **and test areas** (test areas 224) **which are arranged in a common plane** (e.g. top surface of the areas are in a common plane) **and are electrically conductively connected to one another via a conduction web that lies in the common plane** (e.g. conducting web of layer 217 under layer 220, which has a top surfaces that is in the common plane as the test areas and contact areas 222 and 224);

the contact areas being arranged in the passive first region of the top side of the semiconductor chip (contact areas 222 are in the passive region), **the passive first region having no active components of an integrated circuit** (as seen in figure 2, there are no active devices in this region); **and**

the test areas being arranged in the active second region of the top side of the semiconductor chip (test areas 224 are in the active region), **the active second region having active components of an integrated circuit** (e.g. as seen in figure 2, the active second region has a transistor comprising source 204, drain 205, and gate 226); **and**

an insulating layer (insulating layer 216) **having through contacts** (through contact 218) **arranged in the region of the conduction web and extending from the conduction web to a lower plane** (as seen in figure 2), **the through contacts being connected to interconnects that are connected to the components of the integrated circuit** (e.g. vias connected to interconnects 213 and the components of the integrated circuit as described in col. 2, lines 45 - 48);

wherein the contact areas and the test areas are free from the through contacts (as seen in figure 2, the contact and test areas are free from the through contacts);

the semiconductor chip being defined by a boundary around the respective semiconductor chip (e.g. outer boundary as seen in figure 3), **the contact areas and the test areas are completely situated within the boundary of the respective semiconductor chip** (as seen in figure 3, and disclosed in col. 3, line 15 and lines 23 - 26, the test areas and contact areas are within the boundary of the semiconductor chip).

Strauss is silent with respect to explicitly stating that the interconnects are connected to electrodes of the components of the integrated circuit. Strauss does disclose the interconnects are connected to the components of the integrated circuit (col. 2, lines 45 - 48).

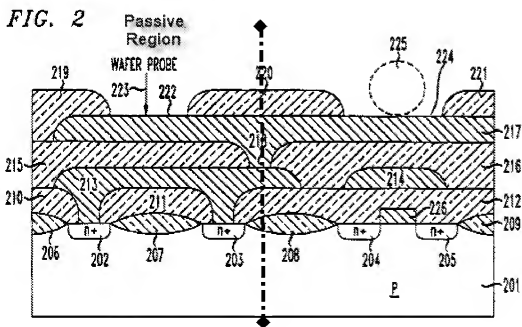
Kim discloses that interconnects within a semiconductor wafer may be connected to electrodes of components of an integrated circuit (e.g. figure 5, interconnects 52 connected to vias connected to the P+ and N+ regions of region 32).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss such that the interconnects are connected to electrodes of the integrated circuit since Strauss discloses the interconnects to be electrically connected to the integrated circuit, and it is well-known in the art that electrodes make the connections between integrated circuits and interconnections, as disclosed by Kim. One would have been motivated to connect the interconnections of Strauss to electrodes of the integrated circuit in order to make an electrical connection, resulting in an operational device.

Strauss is also silent with respect to disclosing the semiconductor wafer comprises a plurality of semiconductor chips.

Kim discloses that semiconductor chips may be formed in plurality on a wafer (e.g. as seen in figures 3 and 4).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Strauss such that there was a plurality of semiconductor chips since it was well-known in the art that a plurality of semiconductor chips are formed on a single wafer, and then separated into individual chips, as disclosed by Kim. One would have been motivated to form a plurality of chips on a single wafer to increase the efficiency of manufacturing by manufacturing several devices simultaneously on a single wafer.



- f. Regarding claim 39, Kim discloses a semiconductor chip (e.g. figures 4 and 5, chip 32) comprising:

a passive first region on a side of the semiconductor chip (region 34);

an active second region on the side of the semiconductor chip
(region 32);

an arrangement of contact areas (contact areas 56b) **and test areas** (test areas 56a) **which are arranged in a common plane** (e.g. as seen in figure 5, the dope surfaces of the contact and test areas are in a common plane) **and are in each case electrically conductively connected to one another via a conduction web that lies in the common plane** (e.g. conducting web 56, which has a top surfaces that is in the common plane as the test areas and contact areas 56a and 56b), **the contact areas being arranged in the passive first region** (contact areas 56b are in the passive region 34), **the passive first region having no active components of an integrated circuit** (as seen in figure 5, there are no active devices in this region), **the test areas being arranged in the active second region** (test areas 56a are in the active region 32), **the active second region having active components of an integrated circuit** (e.g. as seen in figure 5, the active second region has P+ and N+ regions, which are components of an integrated circuit); **and**

an insulating layer situated between the top side and a lower plane
(insulating layer 53, disclosed in col. 3, line 33);

through contacts extending through a portion of the insulating layer below the conduction web (through contacts 55) **and extending from the conduction web to a lower plane** (as seen in figure 5), **the through contacts being connected to interconnects that are connected to electrodes of the**

components of the integrated circuit (e.g. vias connected to the P+ and N+ regions of region 32, and connected to layers 52a and 52);

wherein portions of the insulating layer directly below the contact areas and the test areas are free from the through contacts (as seen in figure 5, portions of the insulating layer 53 directly below the contact and test areas are free from the through contacts).

Kim is silent with respect to disclosing the through contacts extending through a portion of the insulating layer are directly below the conduction web (the conduction web is interpreted as the layer 56 under the insulating layer 57).

Strauss discloses a semiconductor chip (figure 2) **comprising an arrangement of contact areas** (contact areas 224) **and test areas** (test areas 222) **having respective top surfaces which are arranged in a common plane** (e.g. as seen in figure 2, the top surfaces of the contact and test areas are in a common plane) **and exposed to the top side of the semiconductor chip through contact windows and test windows** (windows formed by the absence of layer 219/220/221 on the substrate), **respectively, the contact areas and test areas are in each case electrically conductively connected to one another via a conduction web that has a top surface that lies in the common plane** (e.g. conducting web of layer 217 under the layer 220, which has a top surfaces that is in the common plane as the test areas and contact areas 222 and 224); **an insulating layer situated between the top side and a lower**

plane (insulating layer 216); and through contacts extending through a portion of the insulation layer (through contacts 218) directly below the conduction web and extending from the conduction web to a lower plane (as seen in figure 2), the through contacts being connected to interconnects (interconnects 213).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kim such that the through contacts were formed directly below the conduction web since Kim discloses the through contacts to extend below a side of the conduction web, and Strauss discloses that they may be formed directly below the conduction web. Furthermore, it has been held that rearranging parts of a prior art structure involves only routing skill in the art. *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950). See MPEP 2144.04. One would have been motivated to form the through contact directly below the conduction web in order to avoid damage to the through contact from the formation of a contact on the contact pad.

g. Regarding claim 41, **Kim in view of Strauss discloses the semiconductor chip of claim 18, as cited above, wherein each of the contact areas is electrically conductively connected to a respective one of the test areas by the conduction web extending between and in the same plane as the contact area and the respective test area (Kim: e.g. conducting**

web 56, which has a top surfaces that is in the common plane as the test areas and contact areas 56a and 56b).

h. Regarding claim 42, **Kim in view of Strauss disclose the semiconductor chip of claim 18, as cited above. Kim further discloses a boundary defining the area of the semiconductor chip** (Kim: e.g. as seen in figure 4, chip 32 has a boundary); **a continuous metalized area situated within the boundary** (Kim: e.g. metalized area comprising layer 56, as seen in figure 5); **wherein the contact areas and the test areas are formed on the metalized area** (e.g. as seen in figure 5, contact areas 56b and test areas 56a are formed on the metalized area).

Kim is silent with respect to disclosing the contact areas and the test areas are situated within the boundary of the semiconductor chip.

However, Strauss discloses a boundary defining the area of the semiconductor chip (e.g. as seen in figure 3 of Strauss, the semiconductor chip has an outer boundary); **a continuous metalized area situated within the boundary** (e.g. as seen in figure 2 of Strauss, metalized area comprising layer 217); **wherein the contact areas and the test areas are formed on the metalized area** (contact and test areas 222 and 224, as seen in figure 2 of Strauss), **such that the contact areas and the test areas are situated within the boundary of the semiconductor chip** (Strauss: e.g. as disclosed in col. 3, line 15 and lines 23 – 26).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kim such that the contact areas and test areas were within the boundary of the semiconductor chip since it was known in the art that the chip boundary area may be chosen to include *any* area of the wafer, including an area containing both the test areas and contact areas, as disclosed by Strauss. One would have been motivated to include both the test areas and contact areas within the boundary of the chip in order to allow for further testing of the chip after dicing and separation of the chips from the wafer.

Furthermore, with regard to claims 18 and 42, as cited above, the combination of the Kim reference *in view of* the Strauss reference rendered obvious the claimed invention. However, the Examiner notes that it is the combination of references that renders obvious the claimed invention. As such, the claimed invention as cited in claims 18 and 42 may also be rejected as Strauss *in view of* Kim, where Strauss teaches all of the claimed elements except explicitly the electrodes of the components of the integrated circuit. Since Kim teaches the connection of the interconnects to the electrodes of the components of the integrated circuit, Strauss *in view of* Kim renders obvious the claimed invention. See also the rejection of claim 38.

5. Claims 19, 22 – 25, and 29 – 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Strauss as applied to claims 18 and 28 above, and further in view of Henson (US 6,133,054, prior art of record).

a. Regarding claims 19 and 29, **Kim in view of Strauss discloses the device of claims 18 and 28, as cited above, respectively, wherein the insulating layer (Kim: figure 5, layer 53) is arranged between the components of an integrated circuit (Kim: e.g. N+ and P+ regions in substrate 51) and the test areas of the semiconductor chip (Kim: test areas 56a). Kim is silent with respect to disclosing the insulating layer includes silicon dioxide and/or silicon nitride.**

Henson discloses that insulating layers in semiconductor devices may include silicon dioxide or silicon nitride (col. 4, lines 16 - 23).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kim in view of Strauss such that the insulating layers include silicon dioxide and/or silicon nitride since Kim simply discloses the layers to be insulating, and it was well-known in the art that insulating layers used in semiconductor devices may be formed from silicon oxide or silicon nitride, as disclosed by Henson. Furthermore, it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use silicon dioxide and/or silicon

nitride as an insulating layer since it is a common and easily manufactured insulation material, with well-known properties.

b. Regarding claim 22, **Kim in view of Strauss disclose the semiconductor chip of claim 18, as cited above, but is silent with respect to the interconnects to the electrodes of the components of the integrated circuit comprise copper or a copper alloy.**

Henson discloses that interconnects to electrodes of components of an integrated circuit may comprise copper (e.g. figure 7 shows interconnects 712 and 718, which can comprise copper or copper alloys, as disclosed in col. 4, lines 16 - 23).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use copper for the material of the interconnect structure of Kim in view of Strauss since it was well-known in the art that copper can be used for interconnects in test circuits for integrated circuits, as disclosed by Henson. Furthermore, it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use copper as an interconnect structure since is a low-resistance conductor that is relatively inexpensive.

c. Regarding claim 23, **Kim in view of Strauss disclose the semiconductor chip of claim 18, as cited above, comprising wherein the contact areas and the test areas at their edges and the conduction web on its top side have a insulation and passivation layer** (Kim: layer 57, disclosed col. 3, line 44). **Kim is silent with respect to disclosing the insulating and passivation layer is a multilayer structure.**

Henson discloses that insulation and passivation layers on semiconductor devices may be formed as a multilayer structure (e.g. figure 7, layers 722 and 724, disclosed in col. 4, lines 30 - 32).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the structure of Kim in view of Strauss such that the top insulation and passivation layer comprises multiple layers since Henson discloses a similar device with multiple insulating and passivation layers form atop the device. One would have been motivated to form a multilayer insulation and passivation layer in order to form a multilayer protection layer that is resistant to physical stress, moisture (as discussed in Henson, col. 4, line 30), and is thermally stable.

d. Regarding claim 24, **Kim in view of Strauss, and in view of Henson disclose the semiconductor chip of claim 23, comprising wherein the multilayer insulation and passivation layer includes a layer arranged directly on the edges of the contact areas and of the test areas and on the**

connecting conduction web (e.g. layer 57 of Kim, or layers 722 and 724 of Henson).

Kim, Strauss, and Henson are silent with respect to the layer being silicon dioxide. However, Henson discloses that insulating layers within a semiconductor device may include silicon dioxide (col. 4, line 18).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kim in view of Strauss and Henson such that the insulating layer on the top of the device includes silicon dioxide since Henson discloses that silicon dioxide may be used as insulating layers within semiconductor devices, and it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use silicon dioxide as an insulating layer since it is a common and easily manufactured insulation material, with well-known properties.

e. Regarding claim 25, **Kim in view of Strauss, and in view of Henson disclose the semiconductor chip of claim 23, as cited above, comprising wherein the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer** (Henson: col. 4, lines 22 - 23 and lines 31 - 32).

f. Regarding claim 30, **Kim in view of Strauss, and in view of Henson disclose the electronic device of claim 29, comprising wherein the interconnects to the electrodes of the components of the integrated circuit comprise copper or a copper alloy** (Henson: e.g. figure 7 shows interconnects 712 and 718, which can comprise copper or copper alloys, as disclosed in col. 4, lines 16 – 23).

g. Regarding claim 31, **Kim in view of Strauss, and in view of Henson disclose the electronic device of claim 30, comprising wherein the contact areas and the test areas at their edges and the conduction web on its top side have a multilayer insulation and passivation layer** (e.g. figure 5 of Kim shows insulation and passivation layer 57, and figure 7 of Henson shows a multilayer insulation and passivation layer, including layers 722 and 724, disclosed in col. 4, lines 30 – 32).

Kim, Strauss, and Henson are silent with respect to the multilayer insulation and passivation layer including silicon dioxide. However, Henson discloses that insulating layers within a semiconductor device may include silicon dioxide (col. 4, line 18).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kim in view of Strauss and Henson such that the insulating layer on the top of the device includes silicon

dioxide since Henson discloses that silicon dioxide may be used as insulating layers within semiconductor devices, and it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use silicon dioxide as an insulating layer since it is a common and easily manufactured insulation material, with well-known properties.

h. Regarding claim 32, **Kim in view of Strauss, and in view of Henson disclose the electronic device of claim 30, as cited above, comprising wherein the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer** (Henson: col. 4, lines 22 - 23 and lines 31 - 32).

i. Regarding claim 33, **Kim in view of Strauss and in view of Henson disclose the semiconductor chip of claim 29, as cited above, comprising wherein the conduction web is formed in T** (Kim: e.g. as seen in figure 4, a T is formed from the conduction web 36 at the interface of the test areas and contact areas) **having a transverse bar and a longitudinal bar, the transverse bar of the T having a width about equal to a width of the contact areas** (Kim: e.g. as seen in figure 5, the transverse bar of the T has a vertical width of equal

to the vertical width of the contact area 56b) **and having through contacts to interconnects** (Kim: through contacts 55 to interconnects 52), **while the longitudinal bar of the T has a width determined in response to the maximum current loading during testing by test tips** (the claim limitation of "a width determined in response to the maximum current loading" is not given patentable weight since the patentability of a product does not depend on the method of production. See MPEP 2113. The width of the longitudinal bar of the T exists and the conduction web is capable of supplying current during testing, therefore the structure of Kim in view of Henson anticipates the claimed limitation).

Response to Arguments

6. Applicant's arguments with respect to claims 18, 28, 38, and 39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Huber/
Examiner, Art Unit 2892
November 4, 2009

/Lex Malsawma/
Primary Examiner, Art Unit 2892